REMARKS

Summary of Claim Status

Claims 1, 3-18, and 20-26 are pending in the present application, and are rejected for the reasons discussed below. Applicants respectfully request favorable reconsideration of the claims and withdrawal of the pending rejections and objections in light of the following discussion.

Rejections Under 35 U.S.C. § 102

Claims 1, 3-11, 13-17, 23, and 24 are rejected under 35 U.S.C. § 102(b) as being anticipated by Nicolai, U.S. Patent No. 5,198,707 ("Nicolai"). With respect to Claim 1, the Examiner stated:

> Nicolai discloses (fig 1) a test configuration comprising:
> an integrated circuit to be tested (the structure of figure 1);
> an I/O pad (10) of the integrated circuit;
> an output buffer (13), wherein an output terminal of the output buffer (14) is coupled to the I/O pad (10);
> a current injector (S1) on the integrated circuit coupled to the I/O pad (10) for injecting a current at the I/O pad (10); and
> a detector (column 3 lines 1 – 38) on the integrated circuit coupled to the I/O pad (10) for detecting a logic level (see the abstract) of the I/O pad.

Office Action at page 2. Applicants respectfully disagree and traverse this rejection.

The Examiner has identified element 10 of Nicolai as an I/O pad and element 14 of Nicolai as a buffer. As shown in Figure 1 of Nicolai, the input of buffer 14 is coupled to node C, which is then coupled through a switch S3 to pin 10. Furthermore, the output of buffer 14 is shown connected to a register 16. (See also Nicolai at col. 3, lines 12-16 for further description of the buffer amplifier 14 and its connections.) Thus, the input terminal of buffer 14 of Nicolai, and not its output terminal, is connected (through a switch S3) to pin 10.

In contrast, Claim 1 recites "an output buffer, wherein an output terminal of the output buffer is coupled to the I/O pad." It is clear from Figure 1 of Nicolai that the output terminal of buffer 14 is not coupled to pin 10. Thus, at least this feature of Claim 1 is not taught or disclosed by Nicolai. In fact, Nicolai teaches away from such a

feature since the input of buffer 14 is coupled to pin 10, and having the output of the same buffer coupled to pin 10 would create a useless circuit. Furthermore, the output of buffer 14 in Nicolai needs to be connected to a register for enabling the recording of the logic level present at the node C. See Nicolai at col. 3, lines 12-16. Therefore, Applicants believe Claim 1 is allowable, and allowance of Claim 1 is respectfully requested.

Claims 3-11, 13, and 14 depend, either directly or indirectly, from Claim 1, and thus include all of the limitations of Claim 1. Claim 1 is believed to be allowable for the reasons set forth above. Therefore, Applicants believe Claims 3-11, 13, and 14 are also allowable for at least the same reasons, and Applicants respectfully request allowance of such claims.

With respect to Claim 15, the Examiner stated:

> Nicolai discloses (fig 1) a test configuration comprising:
> . . .
> wherein the current injector is a first transistor (S1) coupled between the I/O pad (10) and a power node (Vcc);
> . . .
> a second transistor (S2) coupled between the I/O pad 910) and a ground node (B);
> a first memory bit (6) coupled to a gate of the first transistor (S1); and
> a second memory bit (7) coupled to a gate of the second transistor (S2).

Office Action at page 5. Applicants respectfully disagree and traverse this rejection.

First, Nicolai does not teach or even suggest that switches S1 and S2 are transistors. Nicolai merely indicates that the switches S1-S4 can be open or closed, and the word "transistor" is never even mentioned in Nicolai. In fact, Nicolai teaches away from switches S1 and S2 being transistors in stating: "the switch S4 is closed and the switches S1, S2, S3 are open. Thus, there is no current consumption possible through the pin 10." Nicolai at col. 3, lines 29-32. As is well-known, transistors have leakage current, even when in an inactive state, and thus if switches S1 and S2 were transistors, current consumption would be possible in Nicolai due to leakage currents in direct contradiction to the statements in Nicolai. In contrast, Claim 15 specifically recites a first and second transistor.

Second, since Nicolai does not teach or suggest transistors of any form, it would be impossible for Nicolai to teach or suggest a gate of a first transistor and a gate of a second transistor. In fact, the terms "transistor" and "gate" are never even mentioned in Nicolai, much less taught or disclosed. Claim 15, in contrast, specifically recites a gate of the first transistor and a gate of the second transistor.

Finally, there is no teaching or suggestion that elements 6 and 7 of Nicolai are memory bits, much less a first memory bit coupled to a gate of the first transistor and a second memory bit coupled to a gate of the second transistor, as recited in Claim 15. In fact, elements 6 and 7 are not even shown connected or coupled to switches S1 and S2, which are alleged to be transistors. Elements 6 and 7 instead appear to be merely inputs to a sequencer for controlling the closing and opening of the switches in a cycle, although that is not even certain since there is no description in the text regarding elements 6 and 7. Those two elements are merely labels attached to arrows pointing into a sequencer and are not referred to anywhere in the text.

Moreover, there is clearly no teaching or suggestion that 6 and 7 of Nicolai are memory bits. In fact, the term "memory" is never even mentioned in Nicolai. Furthermore, 6 and 7 of Nicolai are not shown to be coupled to gates of any transistors, and are only shown connecting to a sequencer.

Therefore, for at least the foregoing reasons, Applicants believe Claim 15 is allowable, and allowance of Claim 15 is respectfully requested.

Claim 16 depends from Claim 15, and thus includes all of the limitations of Claim 15. Claim 15 is believed to be allowable for the reasons set forth above. Therefore, Applicants believe Claims 16 is also allowable for at least the same reasons, and Applicants respectfully request allowance of Claim 16.

With respect to Claim 17, the Examiner stated:

> Nicolai discloses (fig 1) a method for testing an I/O pad of an integrated circuit, the method comprising:
>
> . . .
>
> driving an output value at the I/O pad through an output buffer (14) coupled to the I/O pad (10)

Office Action at page 5. Applicants respectfully disagree and traverse this rejection.

As set forth above in greater detail with respect to Claim 1, the input, and not the output, of buffer 14 of Nicolai is coupled to pin 10. Thus, as shown in the circuit of Figure 1 of Nicolai, it would be impossible to drive an output at pin 10 through buffer 14. In contrast, Claim 17 recites a step of "driving an output value at the I/O pad through an output buffer coupled to the I/O pad." It would be impossible for the circuit disclosed in Nicolai to perform this step since the output of buffer 14 is not even coupled to pin 10. Therefore, Applicants believe Claim 17 is allowable, and allowance of Claim 17 is respectfully requested.

Claims 23 and 24 depend from Claim 17, and thus include all of the limitations of Claim 17. Claim 17 is believed to be allowable for the reasons set forth above. Therefore, Applicants believe Claims 23 and 24 are also allowable for at least the same reasons, and Applicants respectfully request allowance of such claims.

Rejections Under 35 U.S.C. § 103

Claims 12, 25, and 26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Nicolai in view of Rutten, U.S. Patent No. 6,747,469 ("Rutten"). Applicants respectfully disagree and submit that Nicolai and Rutten, alone or in any combination, do not teach or suggest the inventions of Claims 12, 25, and 26. Furthermore, Claim 12 depends from Claim 1, and thus includes all the limitations of Claim 1, and Claims 25 and 26 depend from Claim 17, and thus include all the limitations of Claim 17. Claims 1 and 17 are believed to be allowable for the reasons set forth above. Therefore, for at least the same respective reasons, Applicants believe Claims 12, 25, and 26 are also allowable, and respectfully request allowance of such claims.

Claims 18 and 20-22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Nicolai in view of Fister, U.S. Patent No. 6,285,609 ("Fister"). Applicants respectfully disagree and submit that Nicolai and Fister, alone or in any combination, do not teach or suggest the inventions of Claims 18 and 20-22. Furthermore, Claims 18 and 20-22 depend from Claim 17, and thus include all the limitations of Claim 17. Claim 17 is believed to be allowable for the reasons set forth

above. Therefore, for at least the same reasons, Applicants believe Claims 18 and 20-22 are also allowable, and respectfully request allowance of such claims.

CONCLUSION

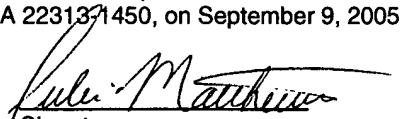
In light of the above remarks, Applicants believe that Claims 1, 3-18, and 20-26 are in condition for allowance, and allowance of the application is therefore requested. If action other than allowance is contemplated by the Examiner, the Examiner is respectfully requested to telephone Applicants' attorney, Justin Liu, at 408-879-4641.

Respectfully submitted,

Justin Liu
Attorney for Applicants
Reg. No. 51,959

I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450, on September 9, 2005.

Julie Matthews
Name



Signature